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S. 1

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/909,489	08/12/97	PEDDLE C	4784.02

LMC1/0429

DORSEY AND WHITNEY
REPUBLIC PLAZA BUILDING
SUITE 4400
370 SEVENTEENTH STREET
DENVER CO 80202-5644

EXAMINER	
PATEL, R	
ART UNIT	**PAPER NUMBER**
2786	7

DATE MAILED: 04/29/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant
08/909,489	Peddle
Examiner	**Group Art Unit**
Ramesh Patel	2786

☒ Responsive to communication(s) filed on *Aug 12, 1997*.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-65* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) *19-49 and 53-64* is/are allowed.

☒ Claim(s) *1-5, 8-16, 50, and 65* is/are rejected.

☒ Claim(s) *6, 7, 17, 18, 51, and 52* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *4, 5 & 6*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 1-65 are presented for examination.

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

3. The information disclosure statements submitted on 1/23/98; 6/4/98 and 12/15/98 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the petition is granted and the information disclosure statement is being considered by the examiner.

Claim Objections

4. Claims 1 and 33 are objected to because of the following informalities: claim 1, line the limitation "amongst" should be "among" and claim 33, line 8, contains the limitation "parts" twice. Applicant is requested to check entire disclosure including all claims and make appropriate correction.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 24, 31 and 65 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 24, recites the limitation "the replacement parts" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 31, recites the limitation "the process", however claim 27 is not a process, rather claim 27 is a module.

Claim 65, it is unclear what the metes and bounds of "any method" are.

Claim Rejections - 35 U.S.C. § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-18, 50-52 and 65 are rejected under 35 U.S.C. 102(b) as being anticipated by Daughton et al.

Daughton teaches the invention (claims 1, 8, 12, 50 and 65) as claimed including a method for developing memory modules using chip parts, and a process for patching with partially defective memory parts to create memory module comprising the steps: testing the part for failed and identifying working segments in the parts is taught as by bit lines test (see col. 4, lines 42-63);

storing the parts according to the results of the testing is taught as the failed chips are stored in groups (see, col. 4, lines 64-68); combining the working segments among different parts, including at least one partially defective parts, in an effective manner to create an effective fully functional transparent memory module is taught as the cells can be combined or substituted by using the redundant line in organizing the defective chips can be made usable (see, col. 9, lines 20-43).

As to claims 2-3, 9-11 and 13-14 Daughton teaches the method and process wherein at least one of the part is package is taught as the memory system uses memory modules containing semiconductor storage arrays having good and defective cells in the package (see, col. 2, lines 18-25).

As to claims 4-5 and 15-16, Daughton teaches the method and process wherein at last one of the parts must be replaced by a substitute part is taught as the memory chips having redundant line for substitution in place of a failing line in the group of cells (see, col. 4, lines 32-41).

As to claims 6-7 and 17-18, Daughton teaches the method and process wherein the patching is done using solder dot connections to provide a logical oring of sets of I/O lines on a printed circuit board is taught as the redundant lines for defective line is accomplished by mounting the chips on one of nine different substrate (see, col. 4, lines 32-68).

8. Claims 51-52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 19-49 and 51-64 are allowable over the prior art of the record.

10. The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 19, 27, 33, 40, 47 and 53, the prior art of the record fails to teach or fairly suggest a memory module and process for selecting primary parts and partially defective parts on a chip on board module comprising a module PC board containing a pattern of solder, the solder dot connections allowing the failing the primary part lines to be replaced by I/O substitute lines from the partially defective parts; wherein the failing line is disconnected from the primary part by removing the solder of its solder dot connection and the substitute line is connected by filling the applicable solder-dot, the substitute line having the equivalent function as the failing line so that the module is transparent to the user; regarding claim 25, method of generating patching instruction traveler chart using optimization, comprising scanning bits of wider parts; identifying unused bits in the smaller parts, wherein the unused bits will be used for substitution; optimizing the selection of the part to use in patching; generating patching instructions; and implementing the generated patching instructions into a traveler chart.

11. Any inquiry concerning this or earlier communication from the examiner should be directed to Ramesh Patel at (703) 308-6673.

If attempts to reach the examiner by telephone are unsucessful, the examiner's supervisor, William Grant, can be reached on (703)308-1108.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

rp
Art Unit-2786
April 23, 1999

PAUL P. GORDON
PRIMARY EXAMINER